# A Novel TDD Mode Direct Conversion Digital Transceiver Using Six-port Technology

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***Abstract* — In this paper, a novel time division duplex (TDD) mode direct digital conversion transceiver using six-port technology is proposed for a QPSK communication. We only use one six-port junction (SPJ) for Tx/Rx mode. To change Tx/Rx mode, we propose a new component, which consists of switched reflection coefficient generator and power detector (SRG&PD). The prototype of the propose six-port transceiver is used to realize the QPSK communication with a 2.4GHz carrier frequency and 10Mbps data rates. Also, the proposed transceiver may be used to low cost, low power consumption and reconfigurable RF systems.**

***Index Terms* — Direct digital conversion, six-port receiver, six-port transceiver, reconfigurable RF system.**

## I. INTRODUCTION

Direct digital conversion transceiver has benefits for modern wireless communications. The main advantage of the direct conversion transmitter is that its transmission contains much less spurious products, which are generated mainly by a mixer, than a super-heterodyne architecture. The direct conversion receiver has no IF and image, thus an expensive IF filter (SAW filter) and image reject filter can be eliminated [1]. Also, due to the increasing the DSP technology, the researches are currently going on reducing signal processing of RF chain [2].

A number of studies of six-port technology have been performed as direct digital conversion receiver architecture, since it can reduce RF signal processing considerably by including not conventional mixer but passive circuit.

The studies of six-port receiver can be classified into the baseband calibration with DSP [3-4], baseband decoder with analog circuit [5-7], and carrier recovery [8]. Also, the six-port transmitter, which is also called by modified vector modulator, was studied [9] and UWB communication using six-port transmitter and receiver is proved its possibility [10]. However, the study on a unified six-port transceiver has not been reported yet.

In this paper, a novel six-port transceiver for TDD mode is proposed. The proposed six-port transceiver use only one six-port junction (SPJ) for Tx and Rx mode. To change Tx/Rx mode, the switching system with the gamma generator and power detector is proposed.

## II. PROPOSED TRANSCEIVER ARCHITECTURE AND OPERATING PRINCIPLE

Fig. 1 shows the block diagram of the SPJ, the conventional six-port transmitter, the conventional six-port receiver and the proposed six-port transceiver. Fig. 1(a) shows a SPJ which is common passive block of the six-port transmitter and six-port receiver. Fig. 1(b) shows the modified reflection type vector modulator, which can be created by changing RF port and LO port of conventional vector modulator [9]. The modulation is achieved by the reflection coefficient which is generated by different termination loads. The modulated signal can be derived as follows:

$$V_{RF} = \frac{1}{2} V_{LO} \sqrt{|\Gamma_I|^2 + |\Gamma_Q|^2} \angle \phi \qquad (1)$$

where $\phi$ is $\tan^{-1}(\Gamma_Q / \Gamma_I)$.

According to Equation (1), QPSK signals can be generated by creating open ($\Gamma$ =1) or short ($\Gamma$ = -1). Fig. 1(c) shows the six-port receiver block diagram. After received signal and the LO reference signal are additive mixed, the power detector converts these mixed RF signal into dc voltages. In the I/Q complex plane, a $\Gamma$ vector can be defined using the four dc output voltages [7]

$$\Gamma = (V_3 - V_4) + j(V_6 - V_5) \qquad (2)$$

where, Vi (i=3,4,5,6) is output dc voltage of the power detector. The I/Q output signals are obtained by using a digital processing or analog baseband signal processing.

Fig.1(d) shows the proposed six-port transceiver topology. One SPJ is shared for Tx/Rx mode and the SRG & PD block operates as the gamma generator at Tx mode and as the power detector at Rx mode. These operating principles make a

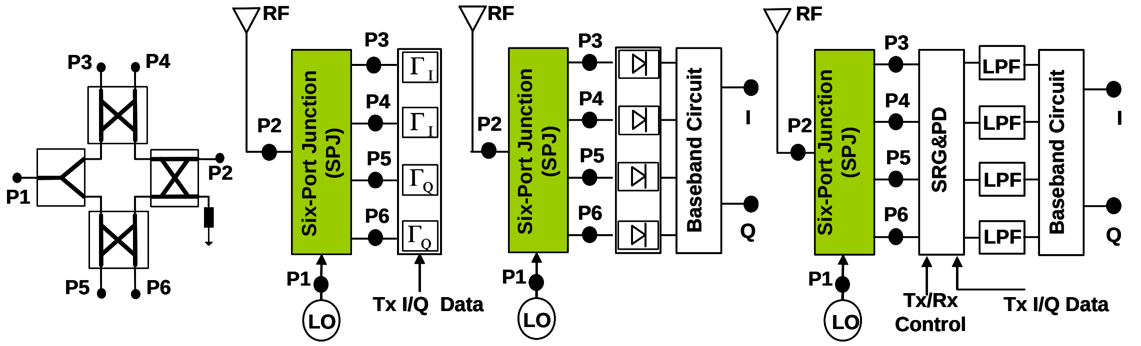



Fig. 1. Block diagram of (a) six-port junction (SPJ), (b) modified six-port transmitter, (c) conventional six-port receiver, (d) proposed six-port transceiver.

possible to operate TDD mode of the proposed six-port transceiver.

## III. Design and Measurement Results

Fig. 1(d) shows proposed six-port transceiver composed of a SPJ, SRG & PD, LPF and baseband decoding circuit. The proposed six-port transceiver board is fabricated and measured using a 0.76 mm thickness and teflon (Er = 3.5) substrate.

### *A. Transceiver design*

The SPJ consists of a Wilkinson power divider and three 90° hybrid couplers. The important parameters of SPJ are input return loss of LO port (S11) and RF port (S22), LO to RF isolation (S21), LO to output port insertion loss (S31, S41, S51, S61). Fig. 2 shows the measured S-parameters of the passive SPJ. At the frequency of 2.4 GHz, the input return losses of LO port, RF port and the isolation of LO to RF exhibit less than -30dB. The insertion losses of the SPJ (LO to P3 or P4) show -6.2dB as expected.

Fig. 3 shows that proposed SRG & PD block diagram. A variable resistance is readily implemented by using the cold bias (Vds=0V) of the pHEMT [11]. For the implementation of the pro-posed SRG & PD, the discrete pHEMT (NE3210-S01) and the power detector (LTC5501-2) are chosen.

In the Tx mode, the baseband digital data is applied to the gate of the pHEMT (Q1) so that the input impedance of the Γ generator is changed. The bias voltage of the gate of pHEMT (Q2) is should be -2 V to turn off Rx path. In the Rx mode, 0V is to be applied to the gate of the both Q1 and Q2, so as to connect RX path and shut down Tx path. As a result, Tx path and Rx path can be switched by controlling the gate voltage of the Q1, Q2, which means TDD mode is possible to implement with the one SPJ and new proposed SRG & PD.

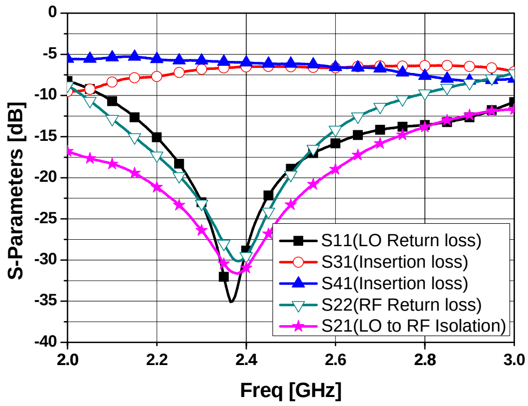



Fig.2. Measured return loss(LO, RF), isolation(LO to RF), insertion loss of SPJ (LO to Port 3 or 4).

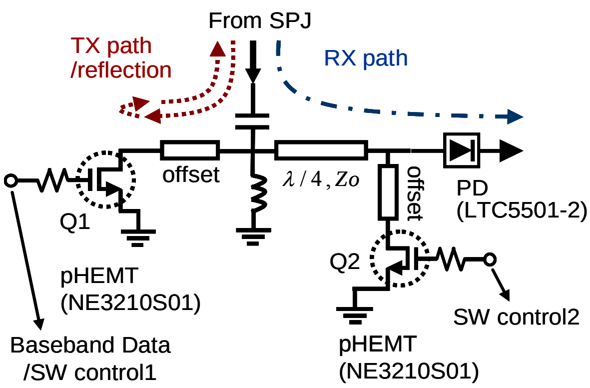



Fig.3. Circuit topology of the switched reflection coefficient generator and power detector (SRG & PD).

The impedance variation at 2.4GHz in the Tx mode by the gate voltage of the Q1 is shown in Fig. 4, which explains ideal short cannot be realized due to the channel resistance of the pHEMT.

Its amplitude and phase difference in aspect of the frequency are also measured to verify the bandwidth at 0V and -2V bias condition of the pHEMT. Fig. 5 indicates that the amplitude error in 2.0 ~ 2.8 GHz is below 1dB which is not very critical effect, but the phase error becomes widely changed even at small frequency variation. This result means QPSK constellation will be distorted by this error factor, even though the constellation is precise at the operating frequency.

For analog baseband decoding circuit of the transceiver on Rx mode, 3-stage instrumentation amplifier is designed using the OPA685 op-amp. The 3-stage instrumentation amp is effective analog decoding circuit obtained I/Q signals according to Equation (2) and its gain is freely adjustable with value of the Rg [12].

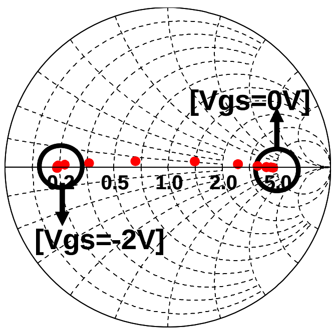



Fig.4. The impedance variation of SRG & PD (2.4GHz) in the TX mode.

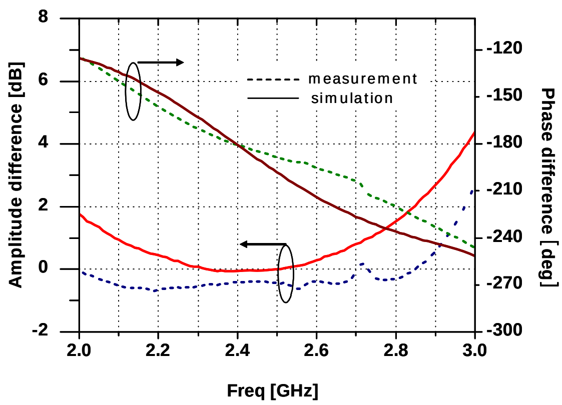



Fig.5. The phase and amplitude difference at 0V and -2V bias in the TX mode.

*B. Six-port transceiver validation*

The test configuration of the proposed six-port transceiver is shown in Fig.7. Two six-port transceivers are used for TX mode and RX mode, respectively.

The signal generator (Agilent E4432A) provides LO signal to two six-port transceivers. LO signal splits in two ways. One is directly fed to transmitter (TX mode), another one is connected to receiver (RX mode) through the phase shifter and attenuator. The phase shifter synchronizes the phase of RF signal with the phase of LO signal and the attenuator is used to adjust difference of the magnitude of RF signal and LO signal. This wired configuration between TX and RX is valid enough to verify the six-port transceiver architecture itself although the real wireless channel is practical case.

For the verification of the TX mode of the six-port transceiver, FPGA board generates pseudorandom bit sequence for the baseband signal, the signal generator provides LO signal. The signal generator generates 5dBm power, so the LO power provided to transmitter is 2dBm while the transmitted power is about -12 dBm. This loss is due to two Wilkinson dividers, the coaxial cable and SMA connector, and mainly because of the -3dB loss of SPG & PD, inherent -3dB loss of the six-port transmitter as shown in Equation (1). The measurement results of TX frequency spectrum exhibits about -12dBm as expected. The modulated frequency spectrums in the case of 5 Mbps and 10 Mbps baseband signal are shown in Fig. 7. The values of various performance versus data rates of 5 Mbps, 10 Mbps, and 15 Mbps are also shown in table I.

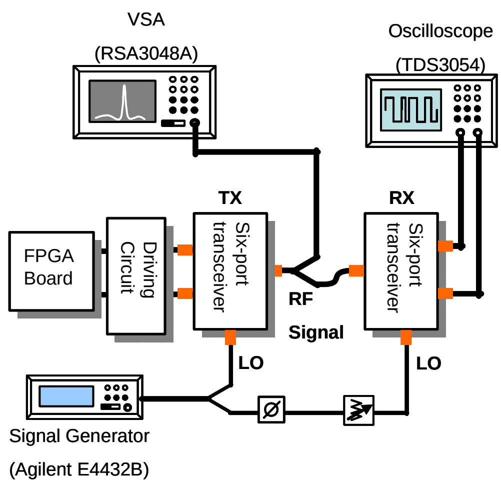
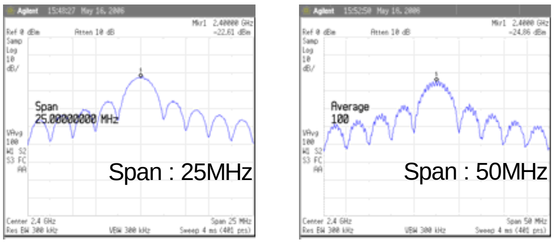


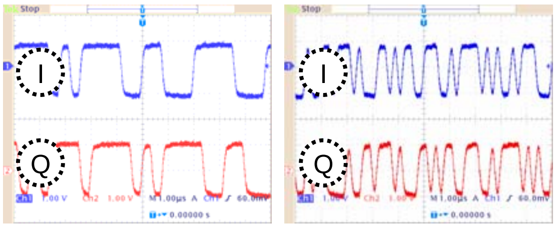

Fig.6. The test configuration of the proposed six-port transceiver

For the verification of the RX mode of the six-port transceiver, received signal is demodulated to the I/Q baseband signal using six-port junction, power detector, and amplified by conventional 3-stage instrumentation amplifier which has 23 dB gain to make 1V p-p signal. The demodulated I/Q signals of 5 Mbps and 10 Mbps are measured by the digital oscilloscope TDS3054, as shown in Fig.8. In the case of 10 Mbps data rates, since the rising time of the signal is almost the same as the bit duration, the shape of the signal exhibits triangle, while in the case 5 Mbps data rate, the demodulated signal is completely recovered. This is why the maximum speed of the power detector (LTC5501-2) is up to 5 Mbps.




(a) (b)

Fig.7. The modulated frequency spectrum (a) 5Mbps (b) 10Mbps.




(a) (b)

Fig.8. The measured demodulated output I/Q waveform (a) 5 Mbps (b) 10Mbps

TABLE I
SUMMARY OF VARIOUS ERRORS VERSUS DATARATE

| | 5Mbps | 10Mbps | 15Mbps |
|---|---|---|---|
| EVM | 1.27% RMS<br>2.32% Peak | 1.86% RMS<br>3.8% Peak | 2.26% RMS<br>4.78% Peak |
| Mag. Error | 0.81% RMS<br>-1.93% Peak | 1.31% RMS<br>3.74% Peak | 1.31% RMS<br>4.16% Peak |
| Phase Error | 0.67deg RMS<br>-1.57deg Peak | 0.76deg RMS<br>-1.74deg Peak | 1.05deg RMS<br>-1.95deg Peak |

## V. CONCLUSION

In this paper, the new six-port transceiver architecture is proposed. This transceiver operates on TDD mode by using the proposed SRG & PD circuit. The results of an experiment on the test bench show good performance for direct conversion transceiver. And the maximum data rate is limited by the gamma generator in the Tx mode and by the speed of the power detector and analog decoding circuit in the RX mode. A low power, low cost and reconfigurable transceiver may be designed by using the proposed six-port transceiver.

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